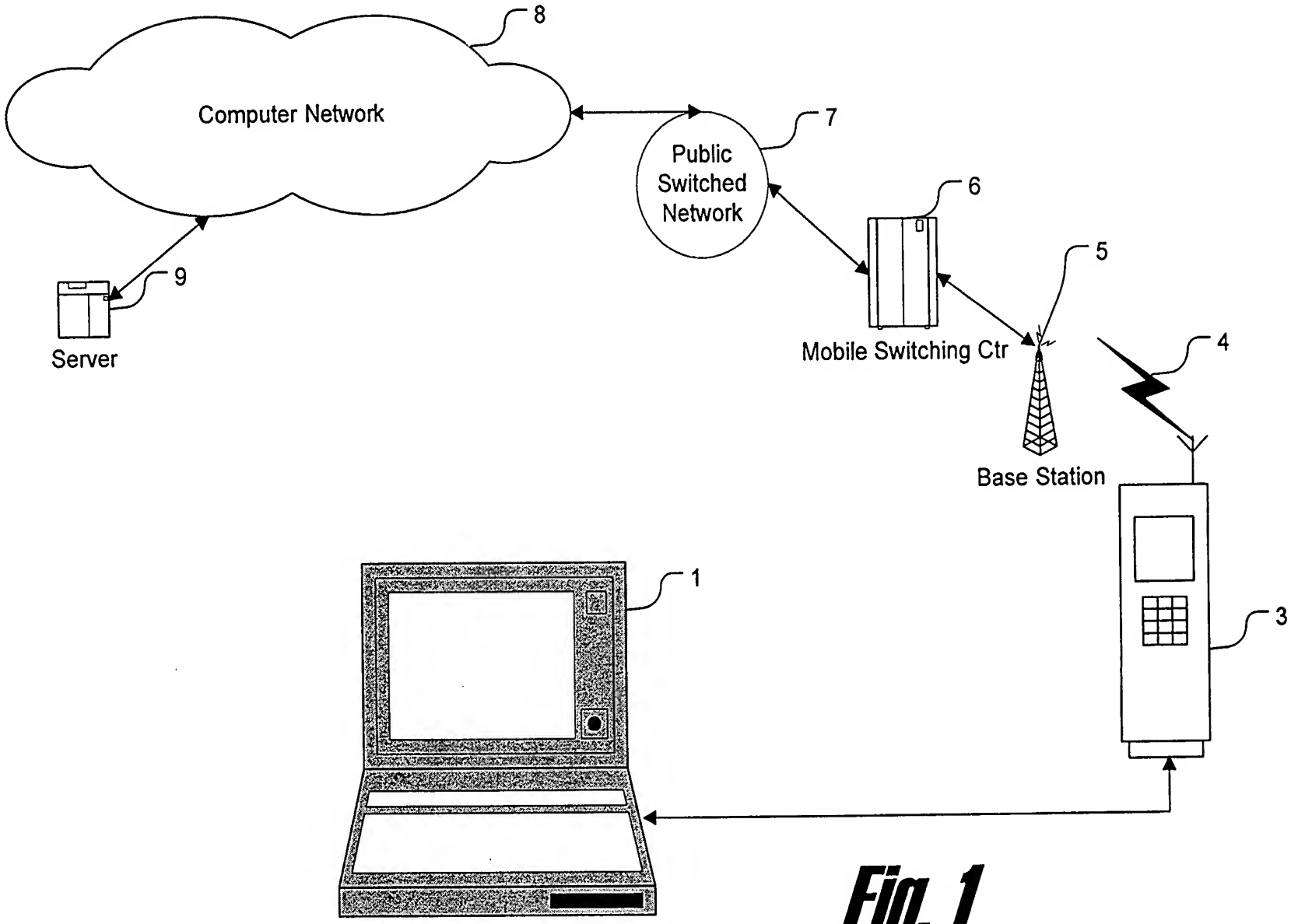
8
Computer Network
7
Public
Switched
Network
6
9
Server
Mobile Switching Ctr
5
4
Base Station
1
3

Fig. 1

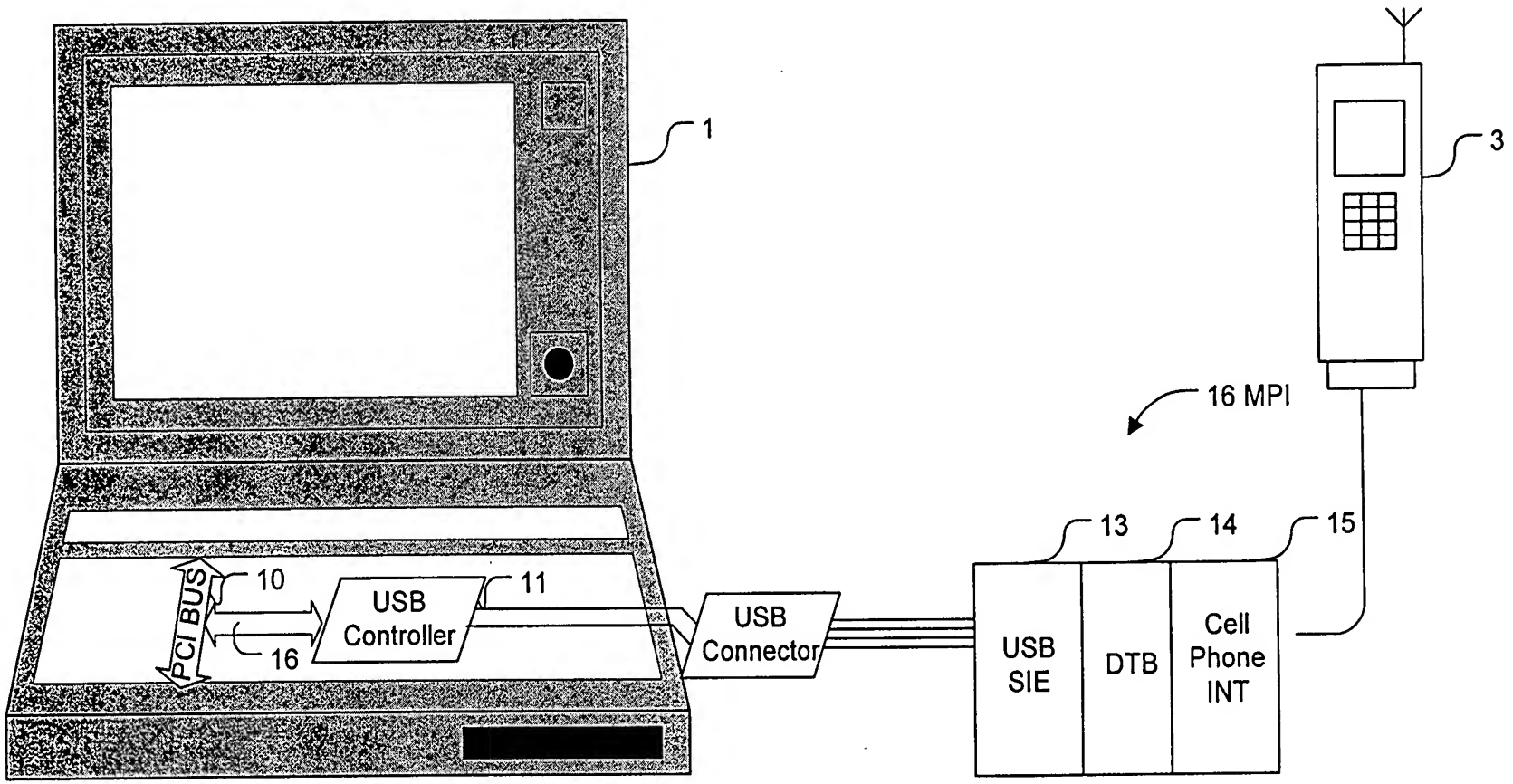
1
3
16 MPI
13
14
15
10
11
16
PCI BUS
USB Controller
USB Connector
USB SIE
DTB
Cell Phone INT

Fig. 2

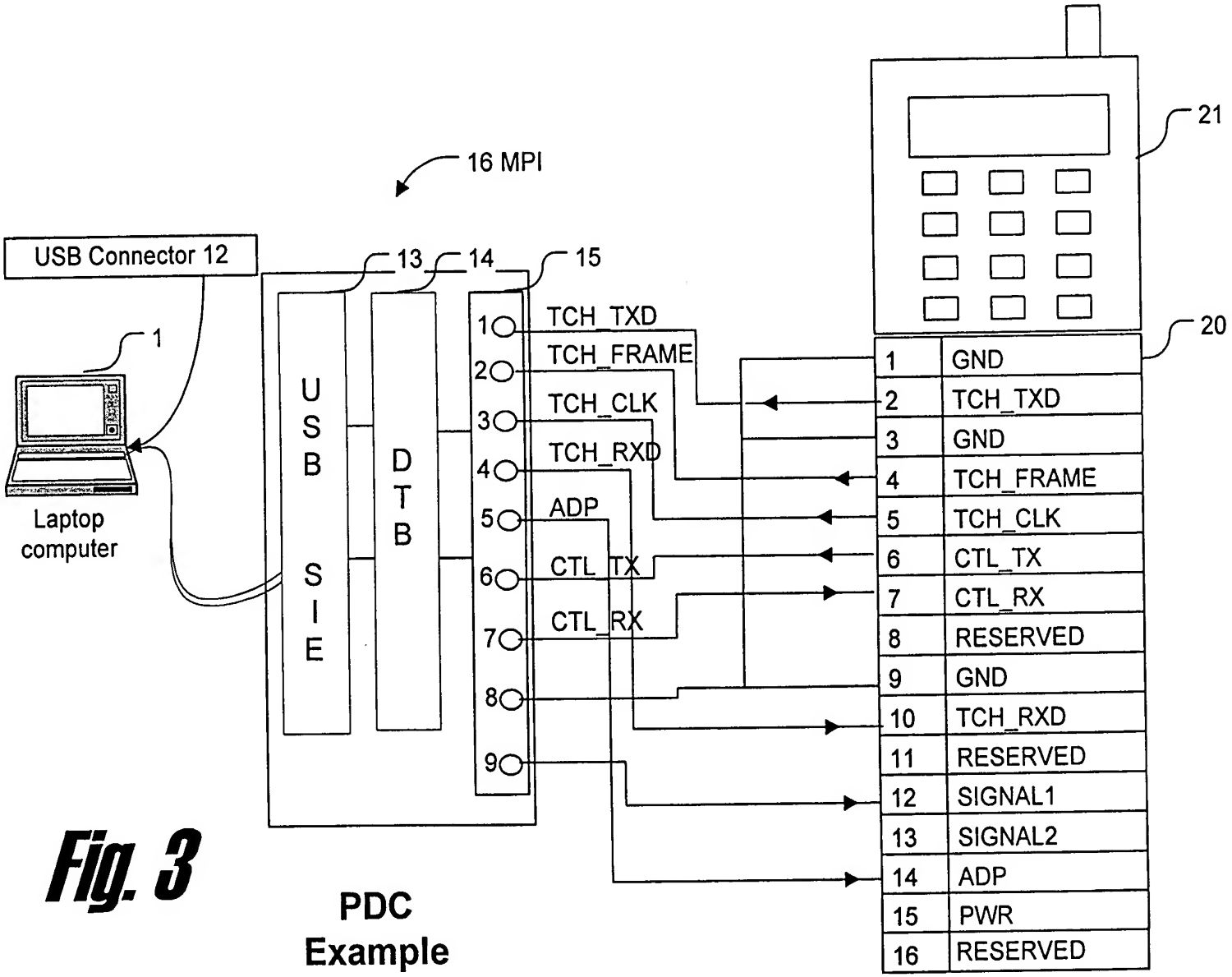


Fig. 3

PDC Example

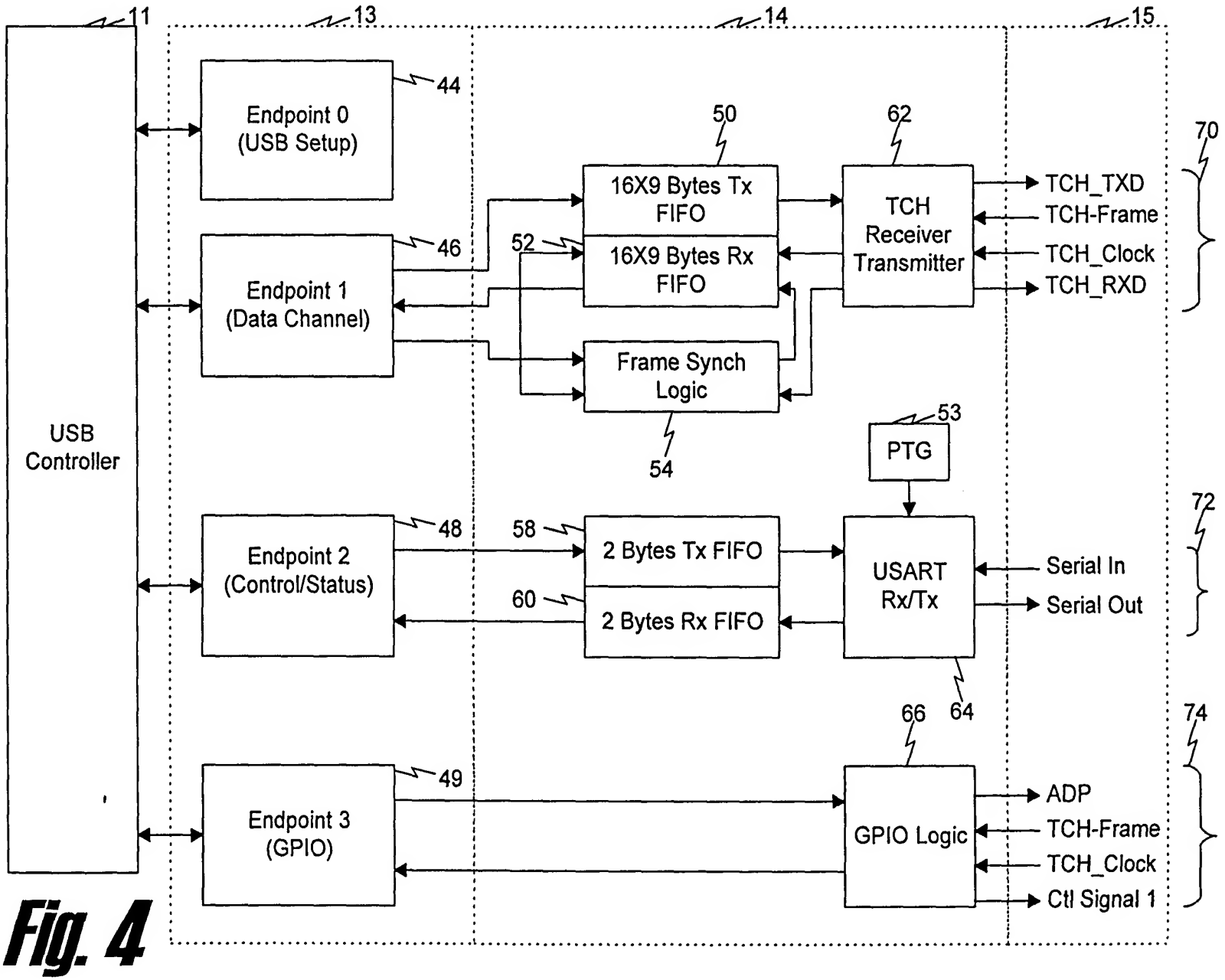
11
13
14
15
USB Controller
Endpoint 0 (USB Setup)
44
Endpoint 1 (Data Channel)
46
Endpoint 2 (Control/Status)
48
Endpoint 3 (GPIO)
49
50
16X9 Bytes Tx FIFO
52
16X9 Bytes Rx FIFO
Frame Synch Logic
54
62
TCH Receiver Transmitter
70
TCH_TXD
TCH-Frame
TCH_Clock
TCH_RXD
53
PTG
58
2 Bytes Tx FIFO
60
2 Bytes Rx FIFO
USART Rx/Tx
64
72
Serial In
Serial Out
66
GPIO Logic
74
ADP
TCH-Frame
TCH_Clock
Ctl Signal 1

Fig. 4

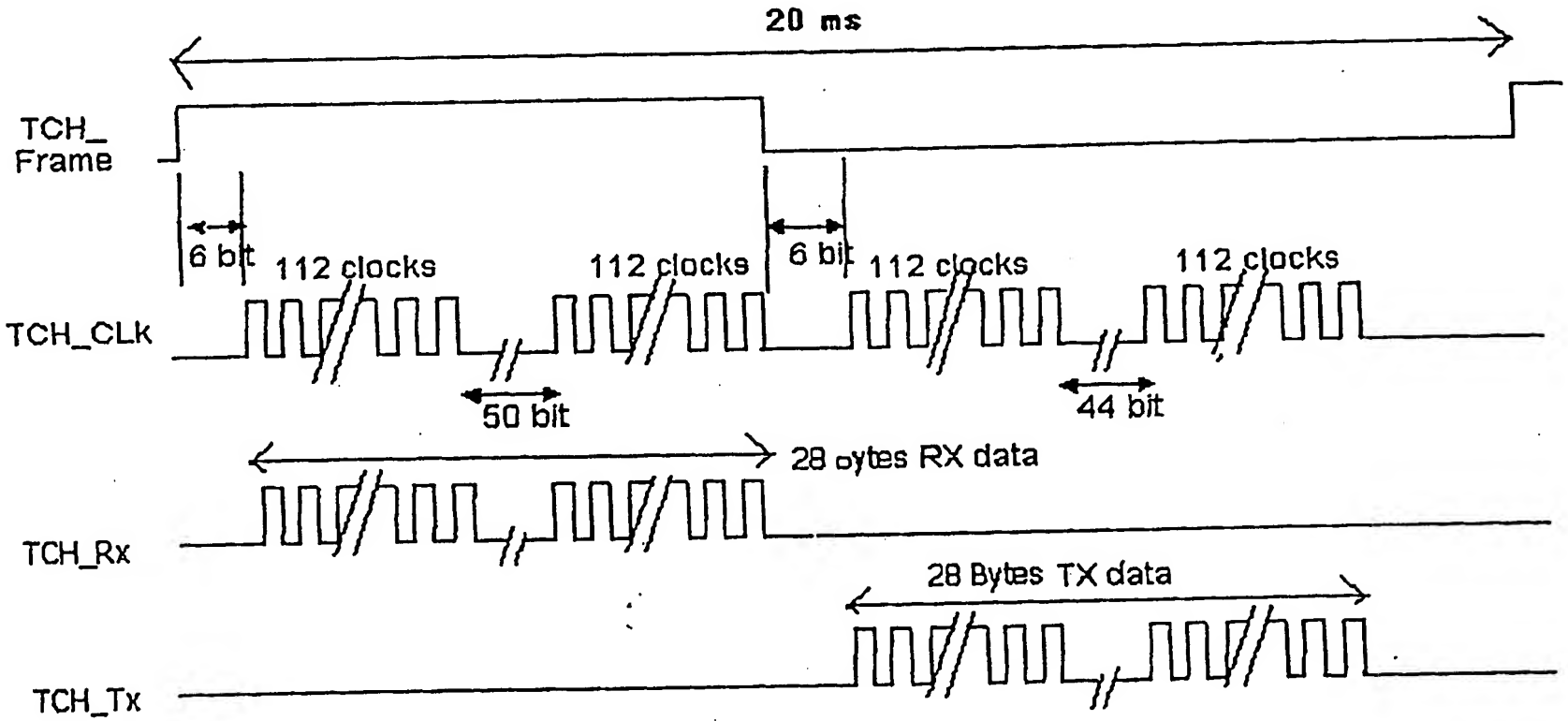
20 ms
TCH_
Frame
6 bit
112 clocks
112 clocks
6 bit
112 clocks
112 clocks
TCH_CLk
50 bit
44 bit
28 bytes RX data
TCH_Rx
28 Bytes TX data
TCH_Tx

Fig. 5

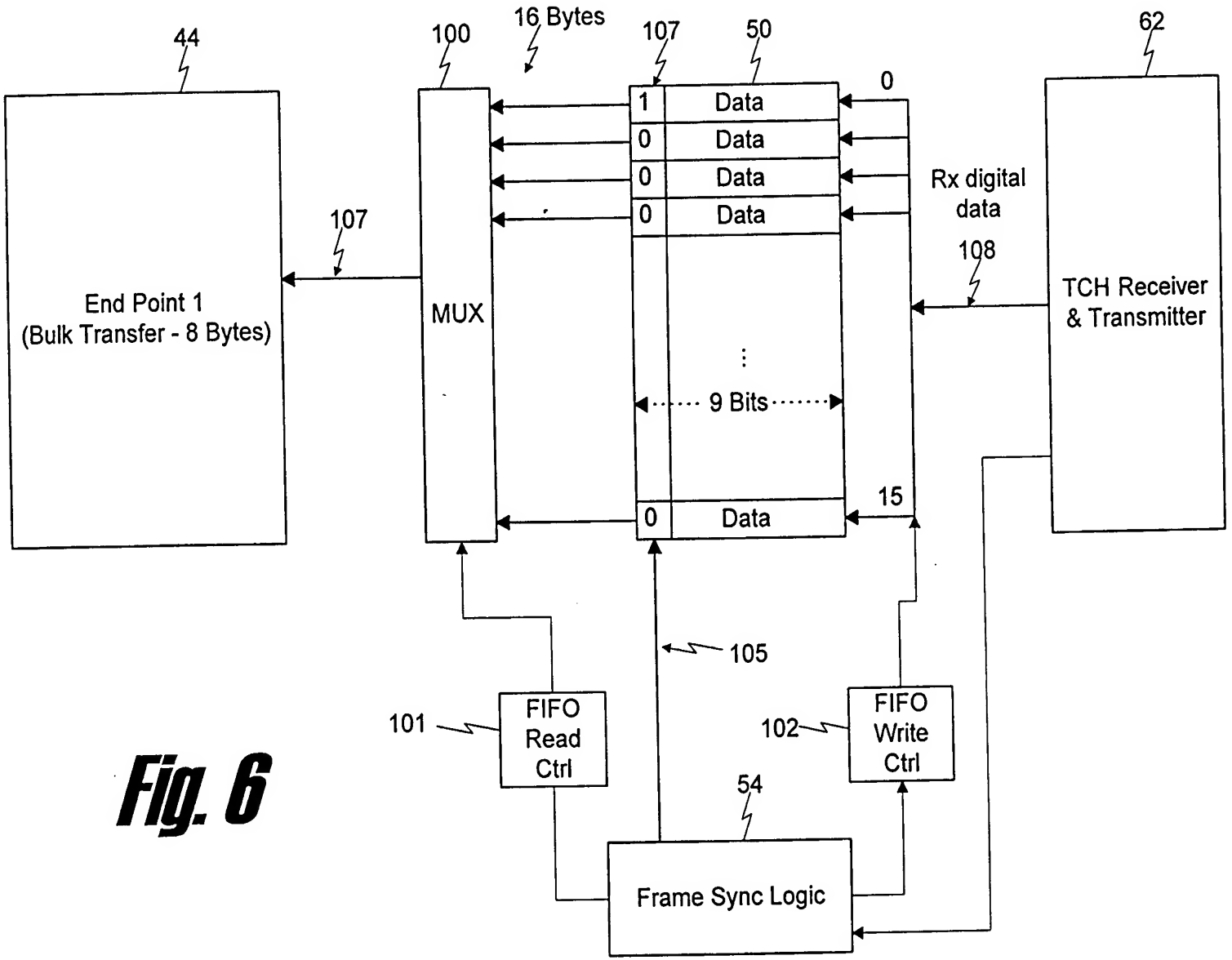
44
100
16 Bytes
107
50
62
0
1
Data
0
Data
0
Data
0
Data
Rx digital
data
108
107
End Point 1
(Bulk Transfer - 8 Bytes)
MUX
TCH Receiver
& Transmitter
9 Bits
15
0
Data
105
101
FIFO
Read
Ctrl
102
FIFO
Write
Ctrl
54
Frame Sync Logic

Fig. 6

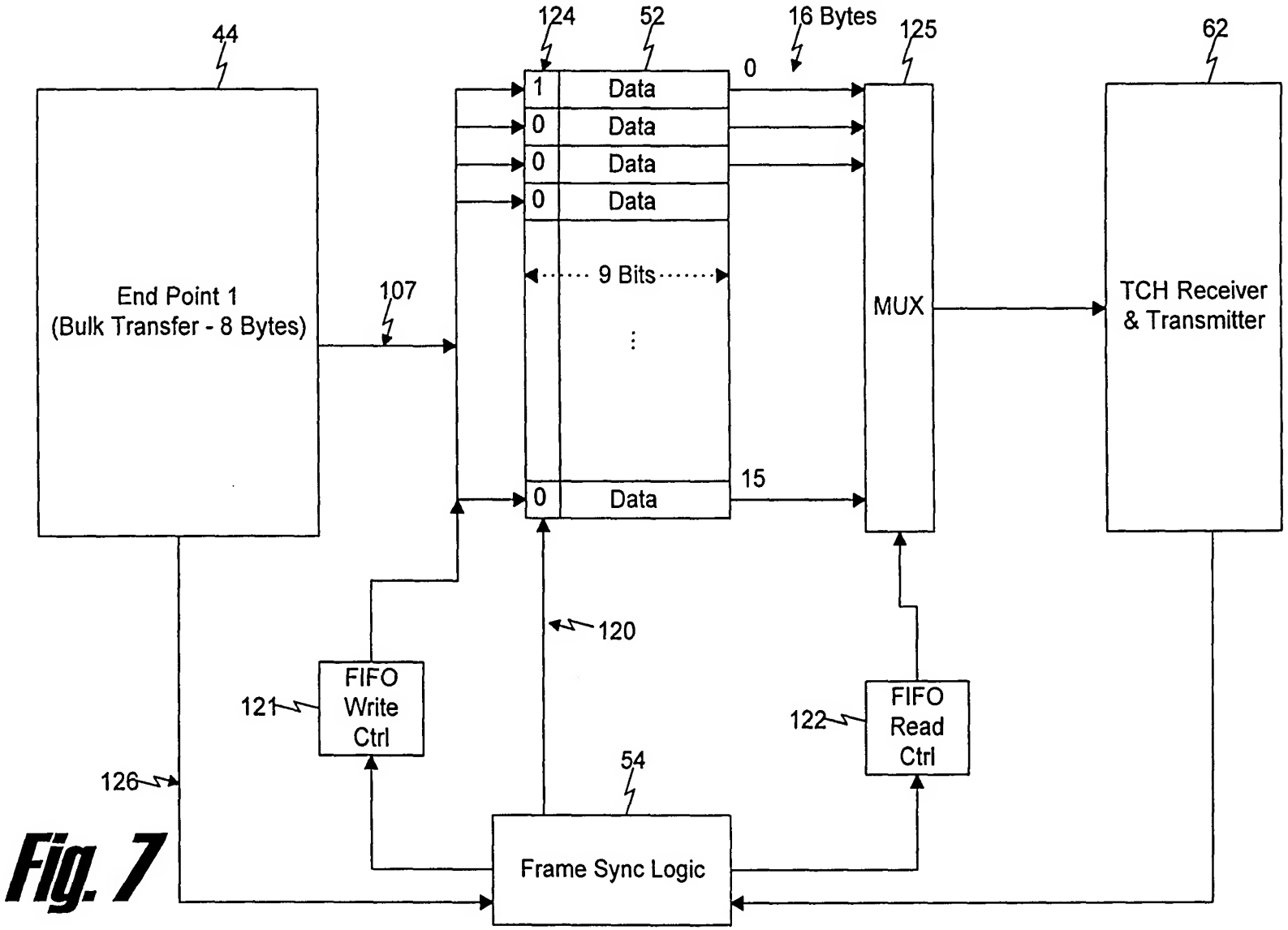
44
124
52
16 Bytes
125
62
1
Data
0
Data
0
Data
0
Data
0
Data
0
Data
End Point 1
(Bulk Transfer - 8 Bytes)
107
9 Bits
MUX
TCH Receiver
& Transmitter
15
120
FIFO
Write
Ctrl
121
FIFO
Read
Ctrl
122
126
54
Frame Sync Logic

Fig. 7

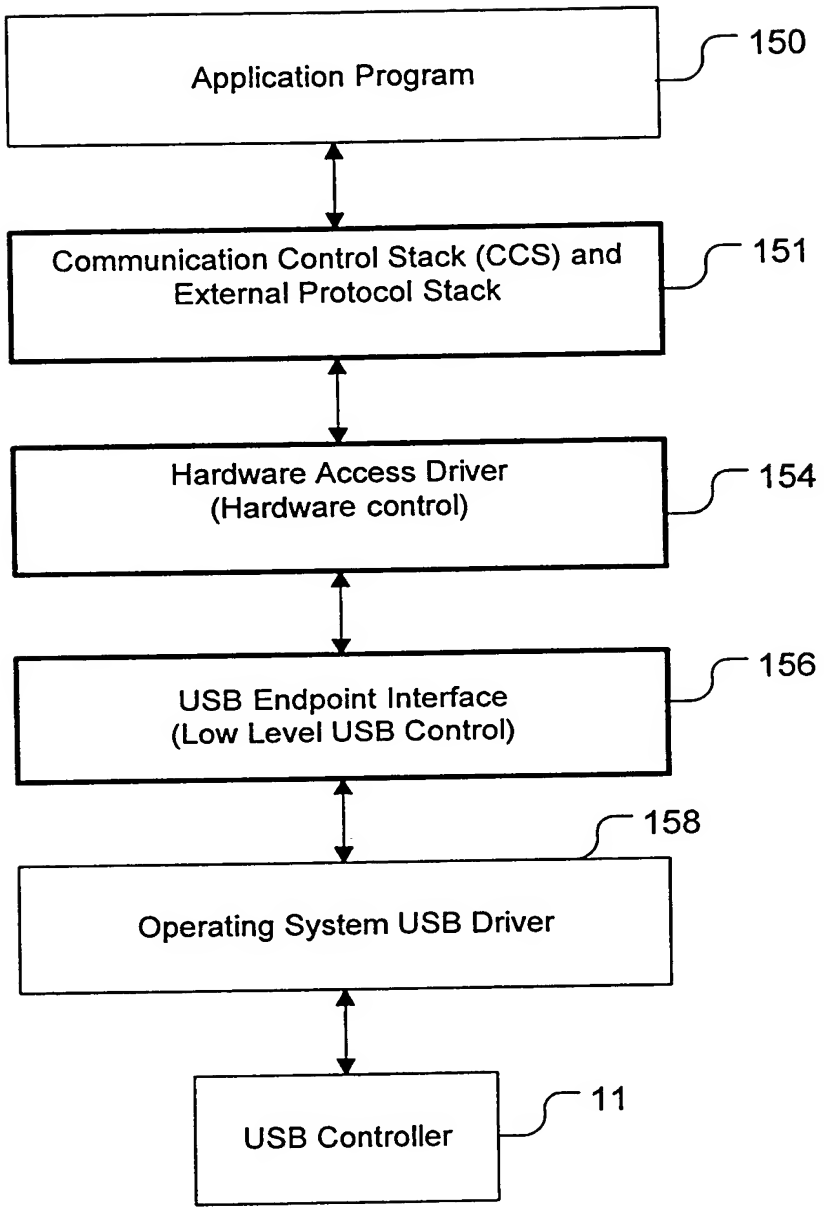
Application Program
150
Communication Control Stack (CCS) and External Protocol Stack
151
Hardware Access Driver (Hardware control)
154
USB Endpoint Interface (Low Level USB Control)
156
158
Operating System USB Driver
USB Controller
11

Fig. 8

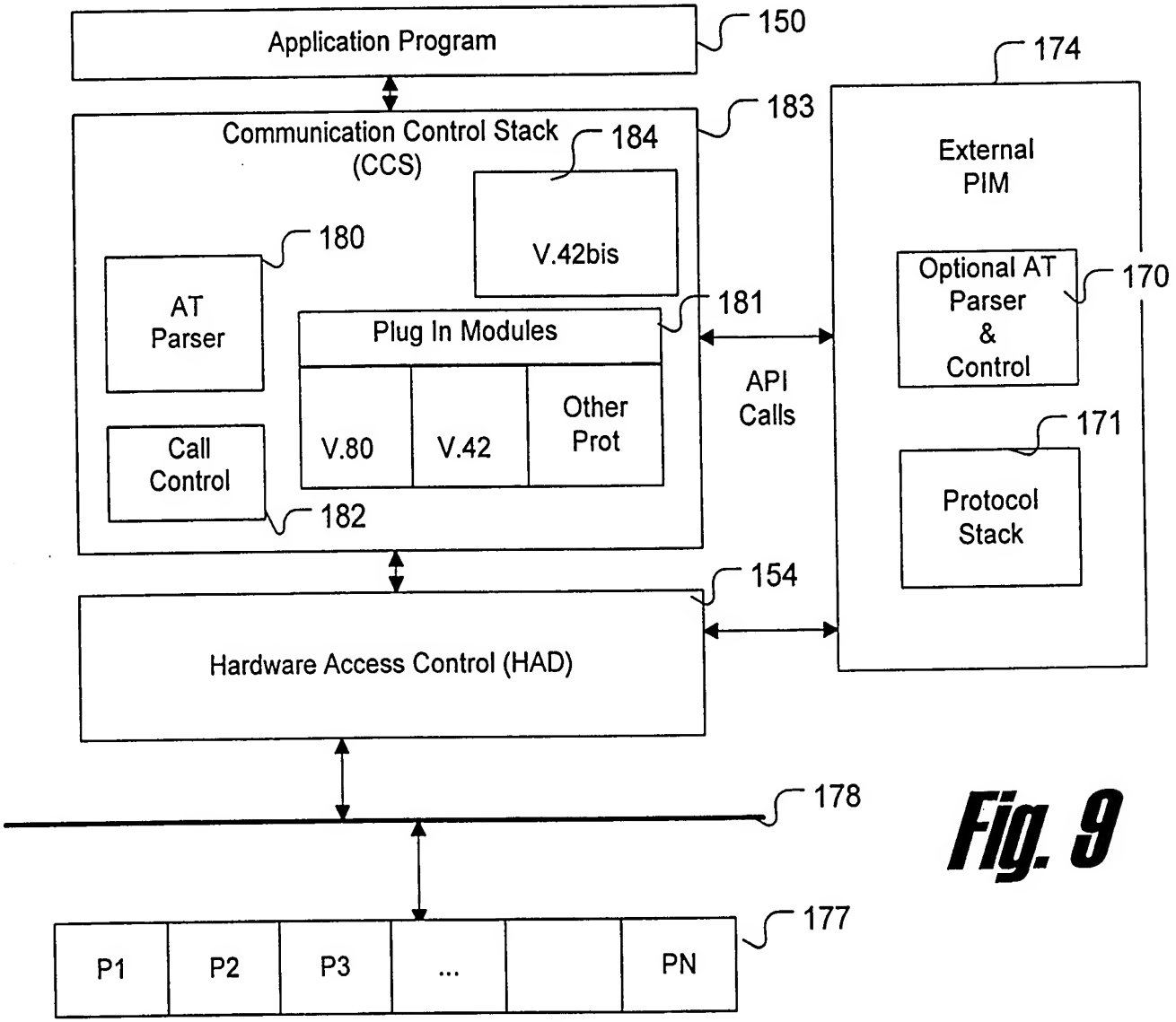
Application Program
150
174
183
Communication Control Stack
(CCS)
184
External
PIM
V.42bis
180
AT
Parser
Optional AT
Parser
&
Control
170
181
Plug In Modules
API
Calls
V.80
V.42
Other
Prot
171
Call
Control
Protocol
Stack
182
154
Hardware Access Control (HAD)
178
177
P1
P2
P3
...
PN

Fig. 9

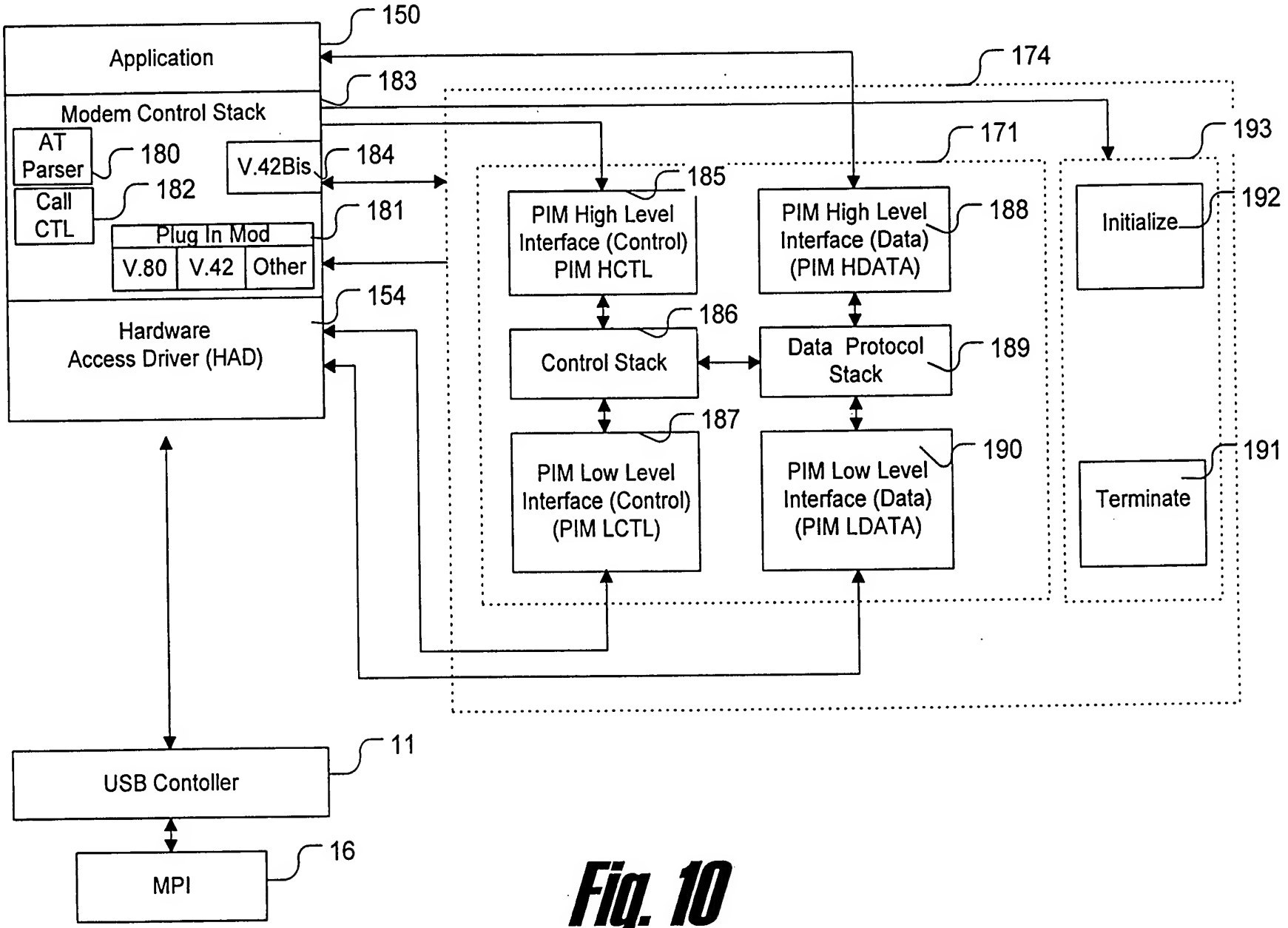
150
Application
174
183
Modem Control Stack
AT Parser
180
V.42Bis
184
Call CTL
182
171
193
185
PIM High Level Interface (Control) PIM HCTL
181
Plug In Mod
V.80
V.42
Other
PIM High Level Interface (Data) (PIM HDATA)
188
Initialize
192
154
Hardware Access Driver (HAD)
186
Control Stack
Data Protocol Stack
189
187
190
191
PIM Low Level Interface (Control) (PIM LCTL)
PIM Low Level Interface (Data) (PIM LDATA)
Terminate
11
USB Contoller
16
MPI

Fig. 10

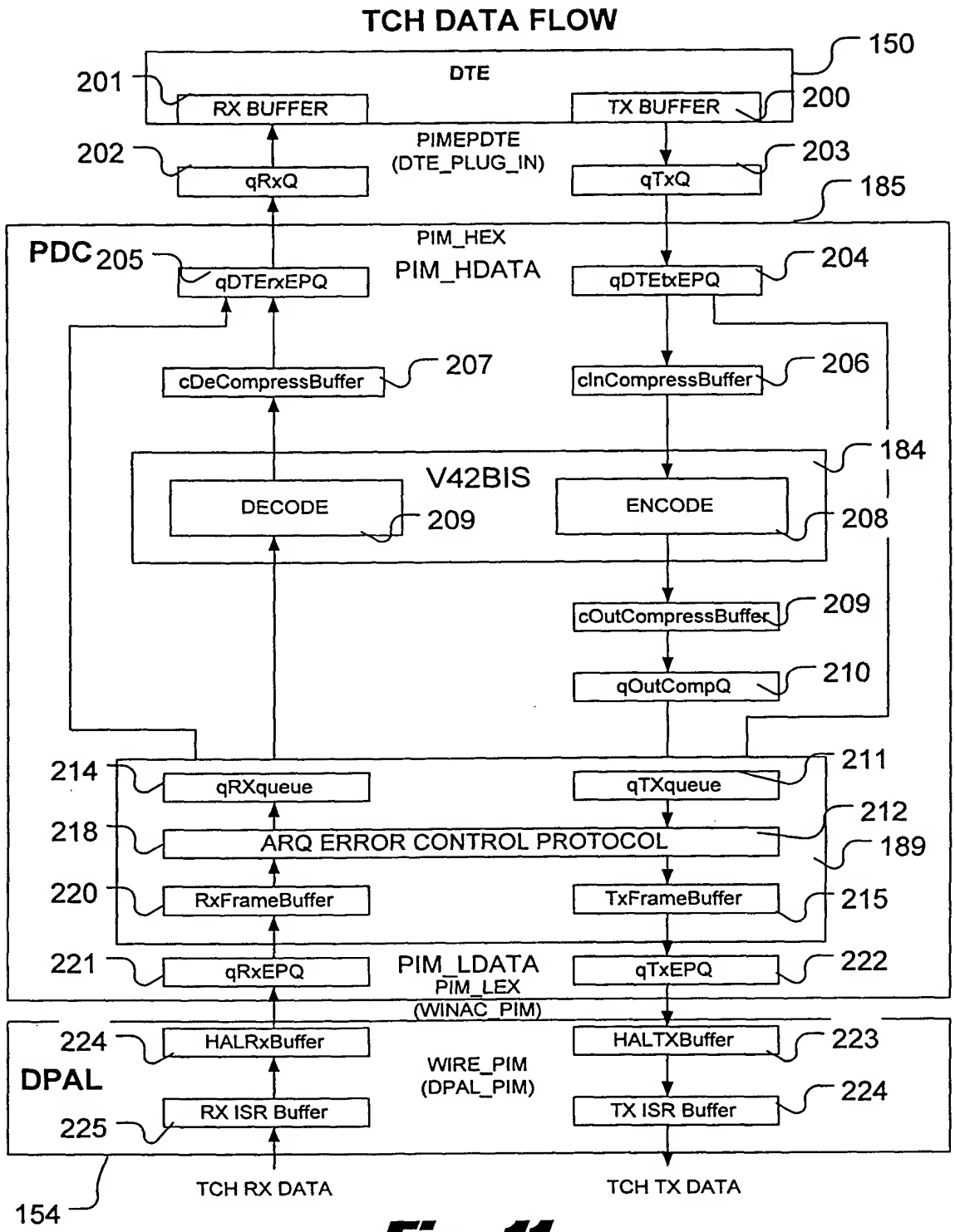
TCH DATA FLOW
DTE
150
201
RX BUFFER
TX BUFFER
200
PIMEPDTE
(DTE_PLUG_IN)
202
qRxQ
qTxQ
203
185
PIM_HEX
PDC
205
PIM_HDATA
qDTErxEPQ
qDTEtxEPQ
204
cDeCompressBuffer
207
clnCompressBuffer
206
184
V42BIS
DECODE
209
ENCODE
208
cOutCompressBuffer
209
qOutCompQ
210
214
qRXqueue
qTXqueue
211
212
218
ARQ ERROR CONTROL PROTOCOL
189
220
RxFrameBuffer
TxFrameBuffer
215
221
qRxEPQ
PIM_LDATA
PIM_LEX
(WINAC_PIM)
qTxEPQ
222
224
HALRxBuffer
HALTXBuffer
223
DPAL
WIRE_PIM
(DPAL_PIM)
225
RX ISR Buffer
TX ISR Buffer
224
154
TCH RX DATA
TCH TX DATA

Fig. 11

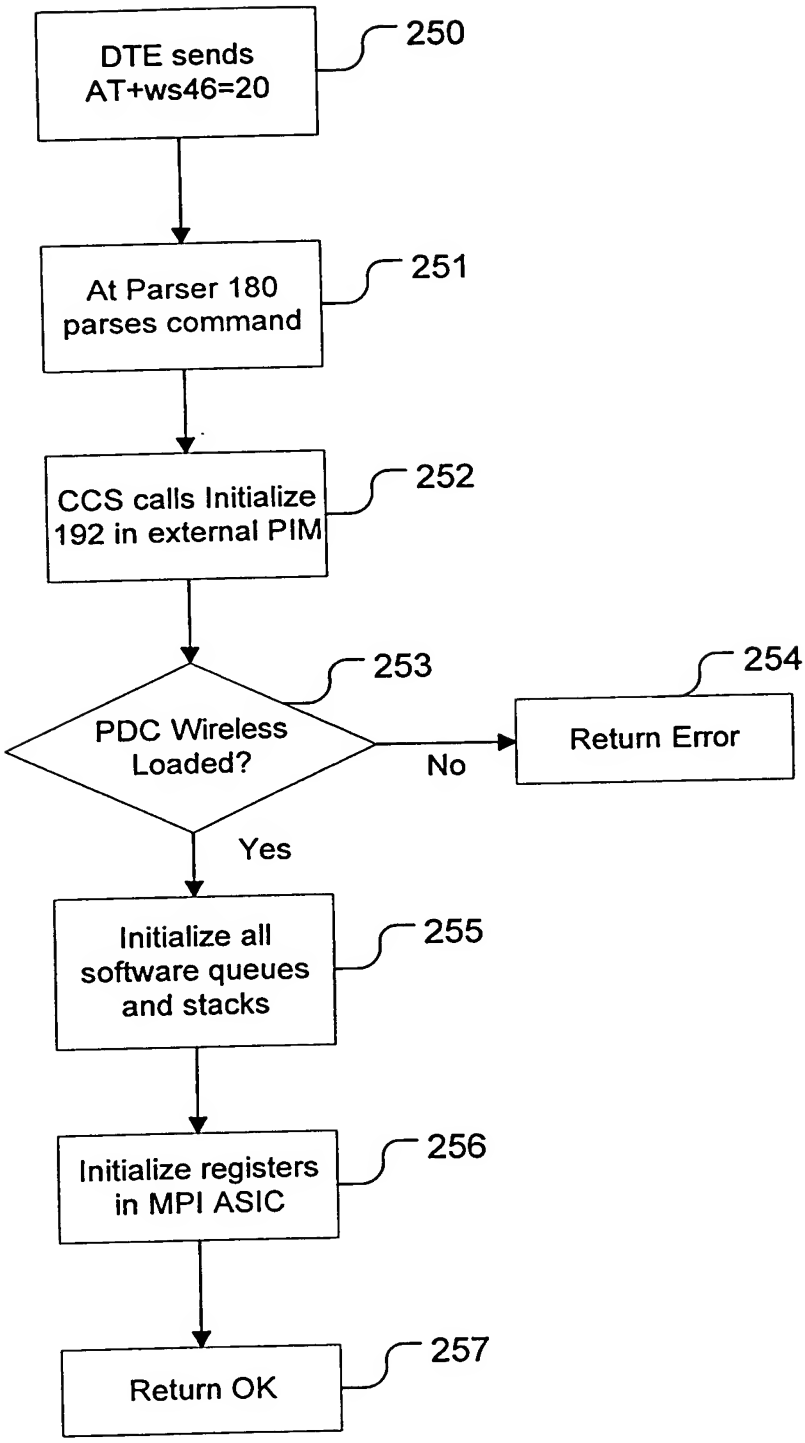
DTE sends AT+ws46=20
250
At Parser 180 parses command
251
CCS calls Initialize 192 in external PIM
252
PDC Wireless Loaded?
253
No
Return Error
254
Yes
Initialize all software queues and stacks
255
Initialize registers in MPI ASIC
256
Return OK
257

Fig. 12

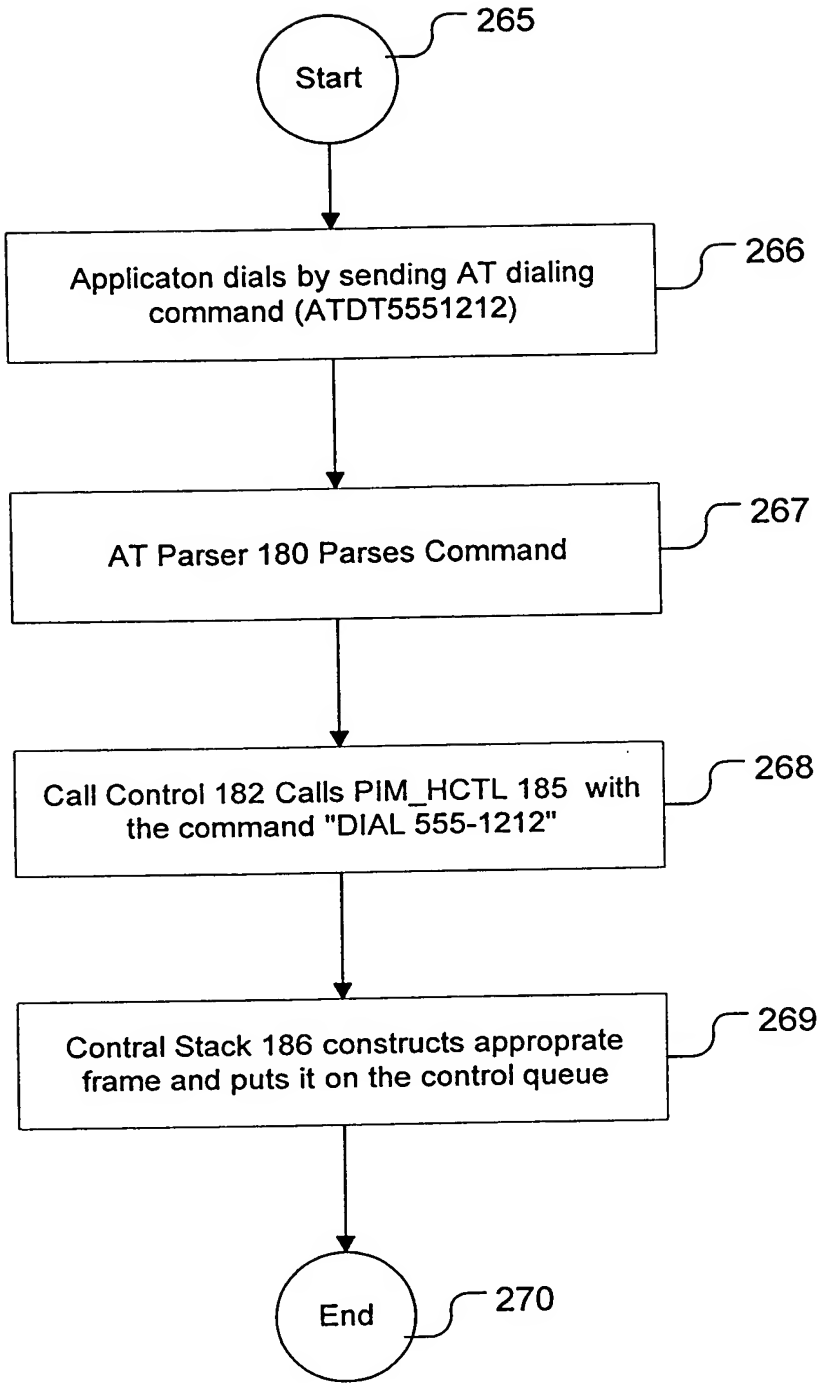


**Fig. 13A** Control Flow High Level

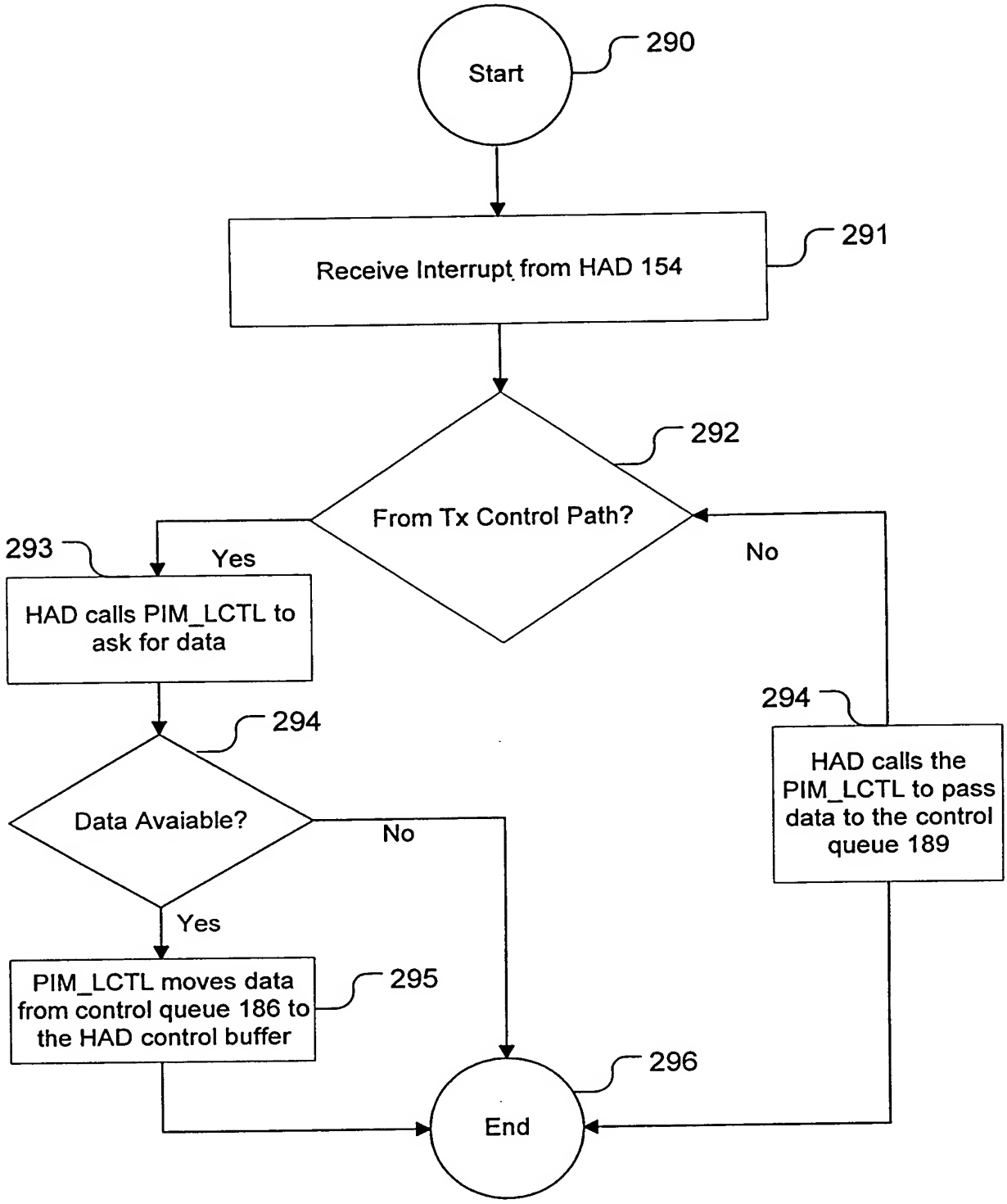


**Fig. 13B** Control Flow Low Level

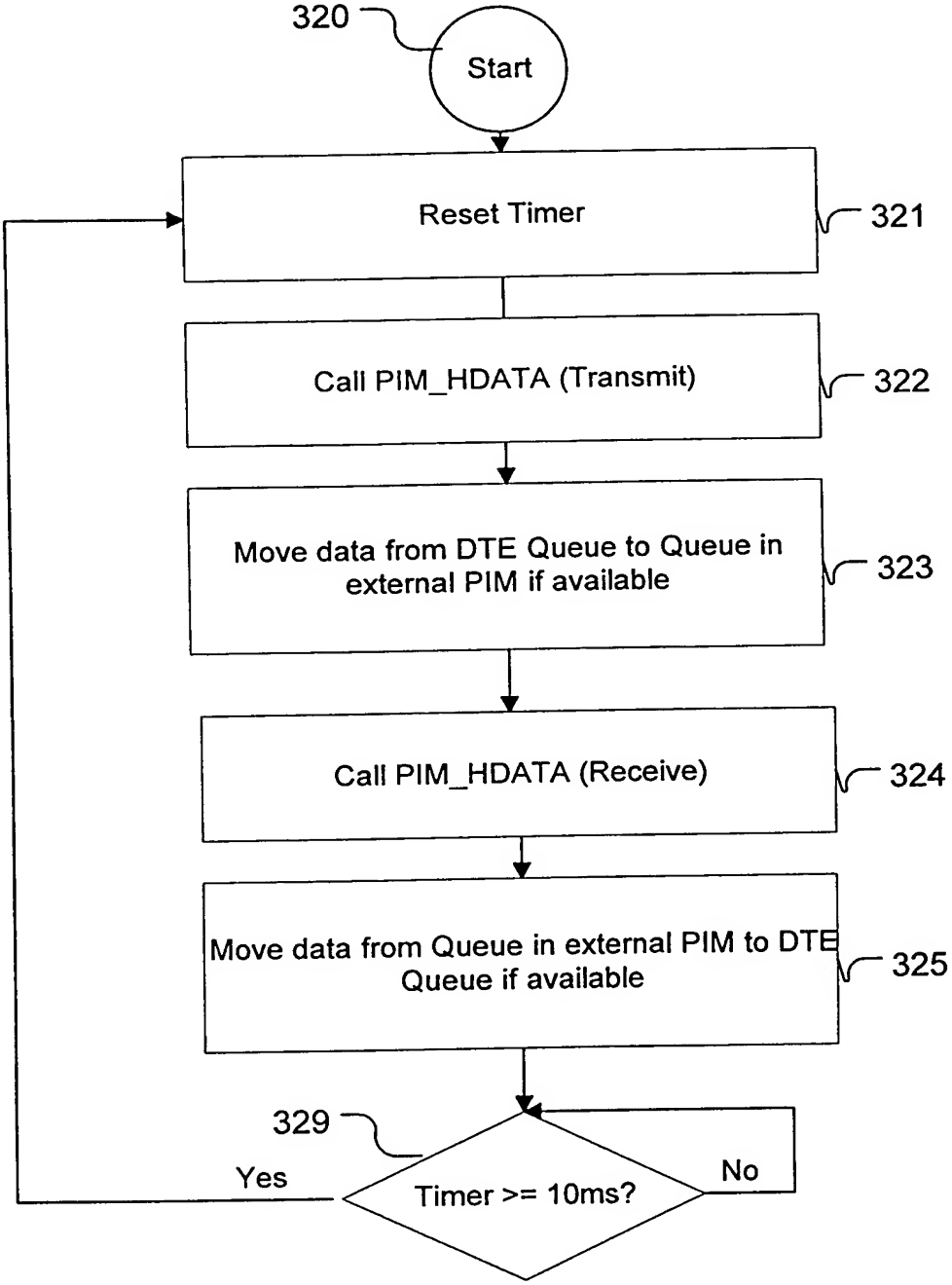


FIG. 14A Data Flow High Level

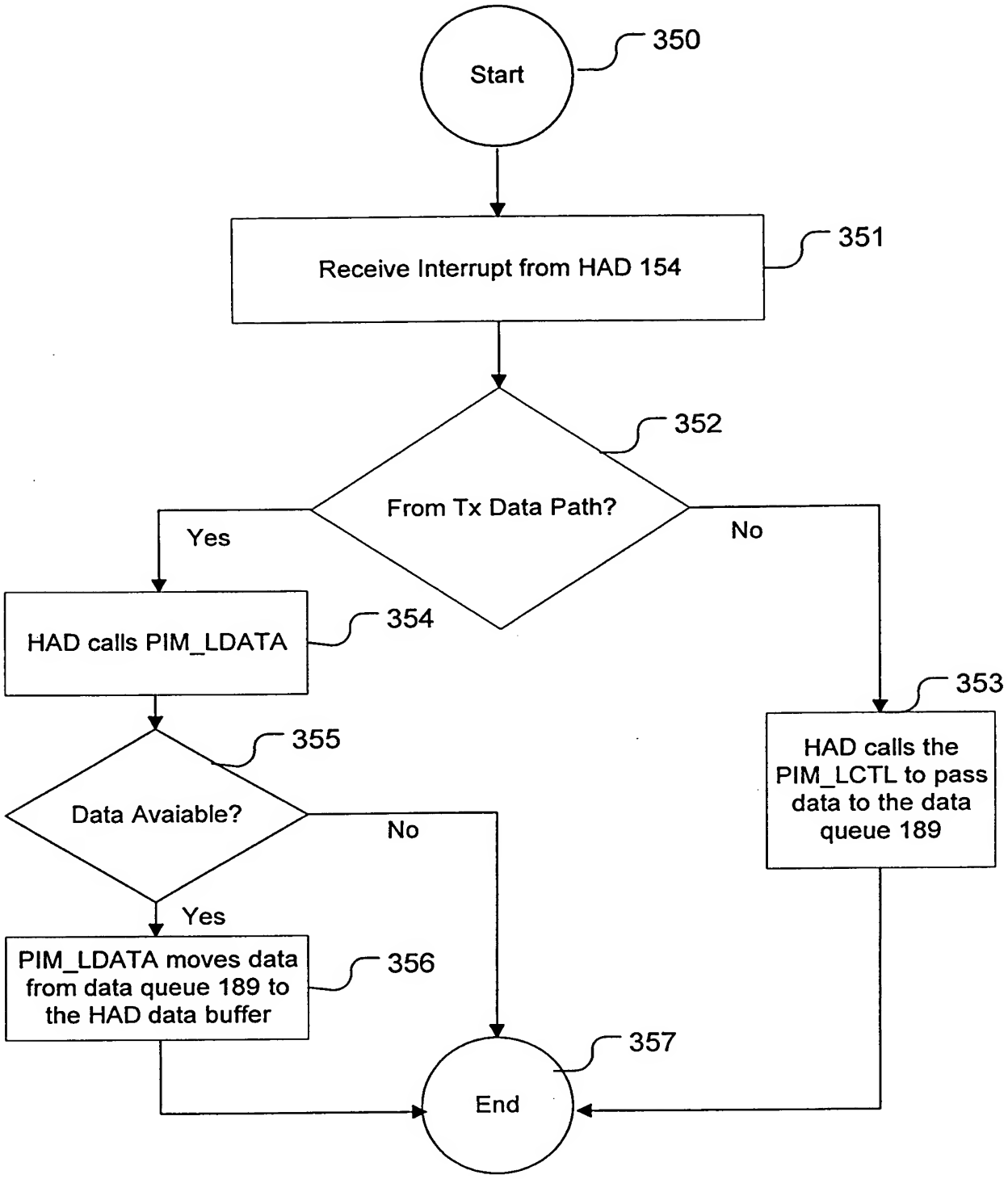


**Fig. 14B** Data Flow Low Level